

The diagram illustrates a liquid crystal display panel structure. It features a grid of pixels (PXL) within a peripheral pad (PP) region. A common data line, labeled 1B, runs horizontally across the panel. Each pixel (PXL) contains subpixels 1, 2, and 3. A voltage source Vw is connected to the bottom edge of the panel. The label 5 indicates the substrate. The PXA label points to the pixel array region. The diagram shows a series of pixels connected to the common data line 1B, with subpixels 1, 2, and 3. The voltage source Vw is connected to the bottom edge of the panel.

FIG. 1C

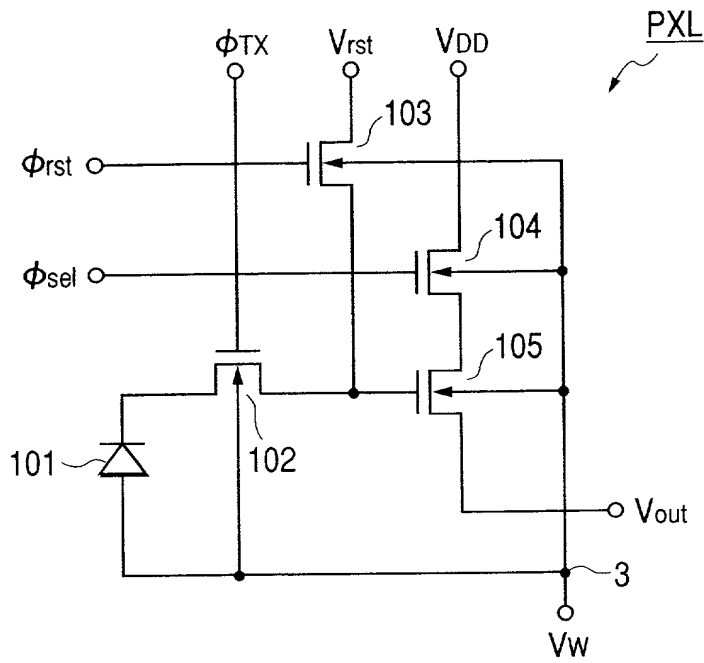
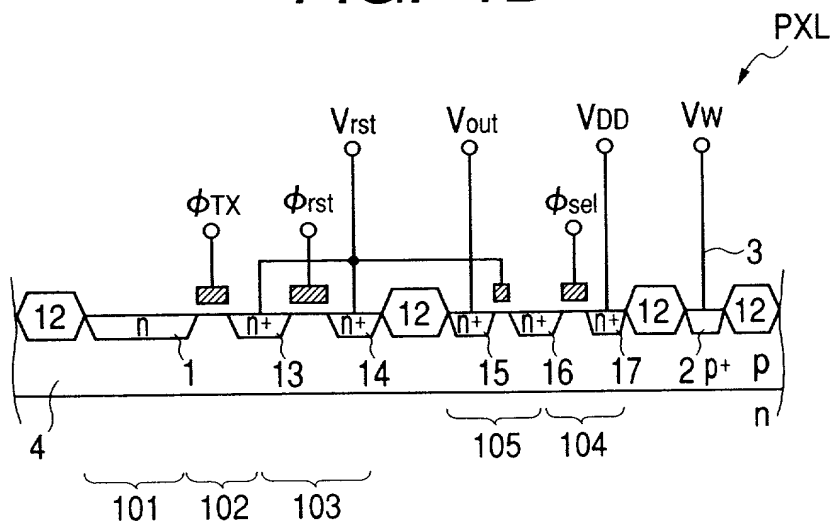
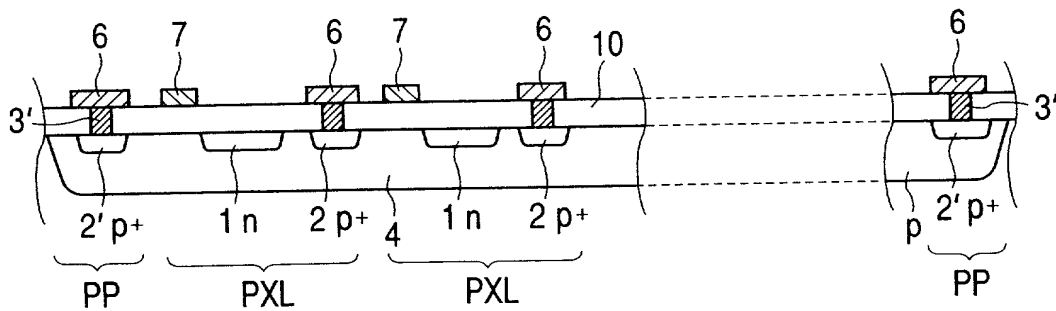


FIG. 1D



**FIG. 2B**



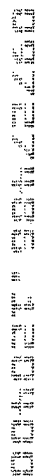
[illegible]

FIG. 4A

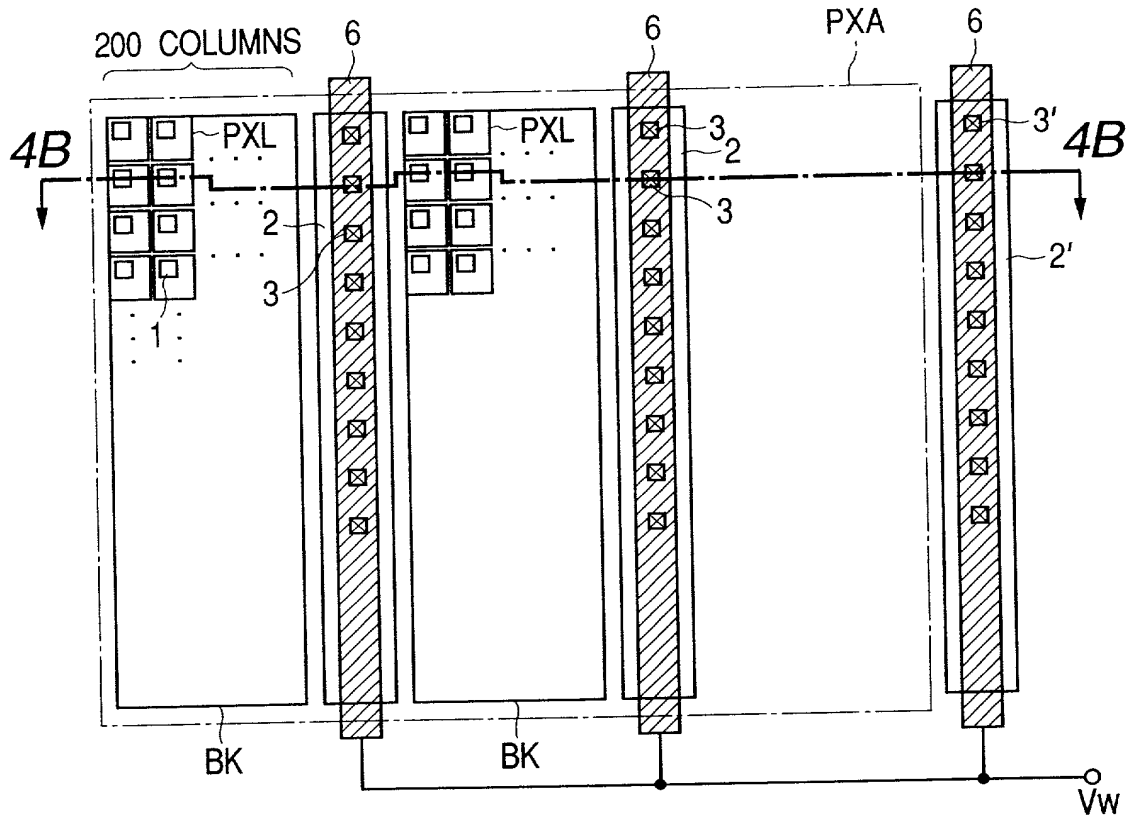


FIG. 4B

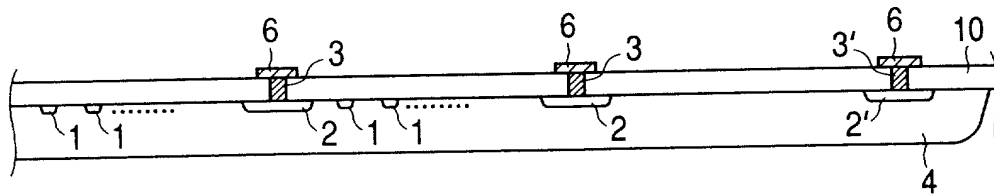
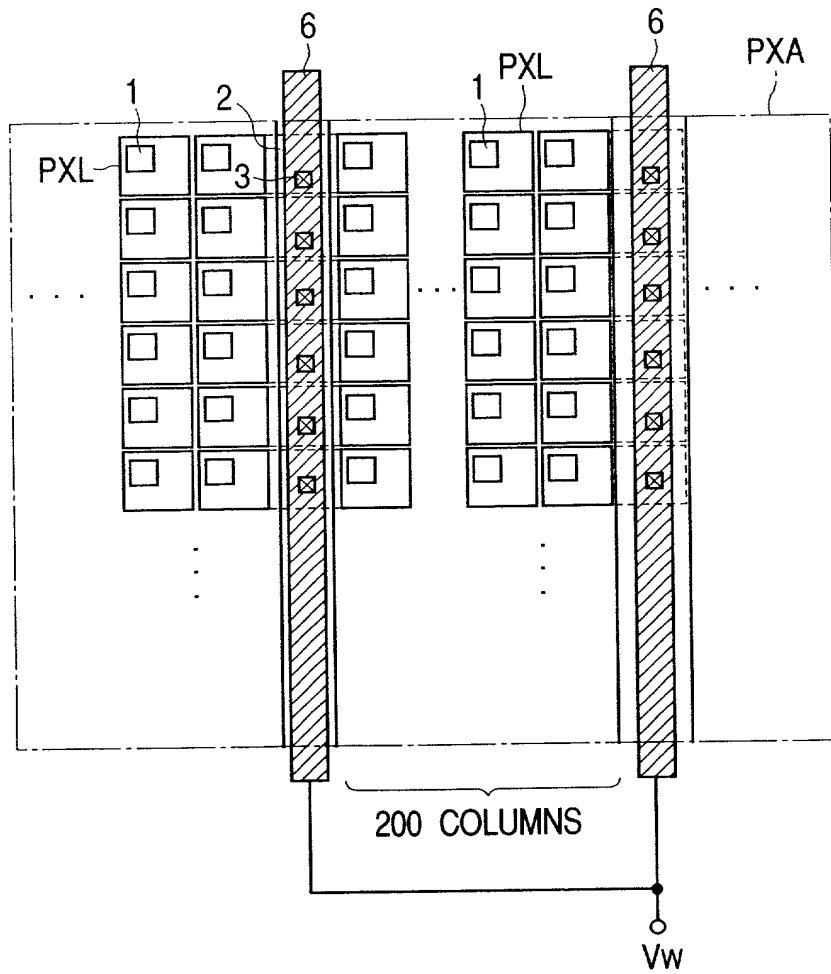
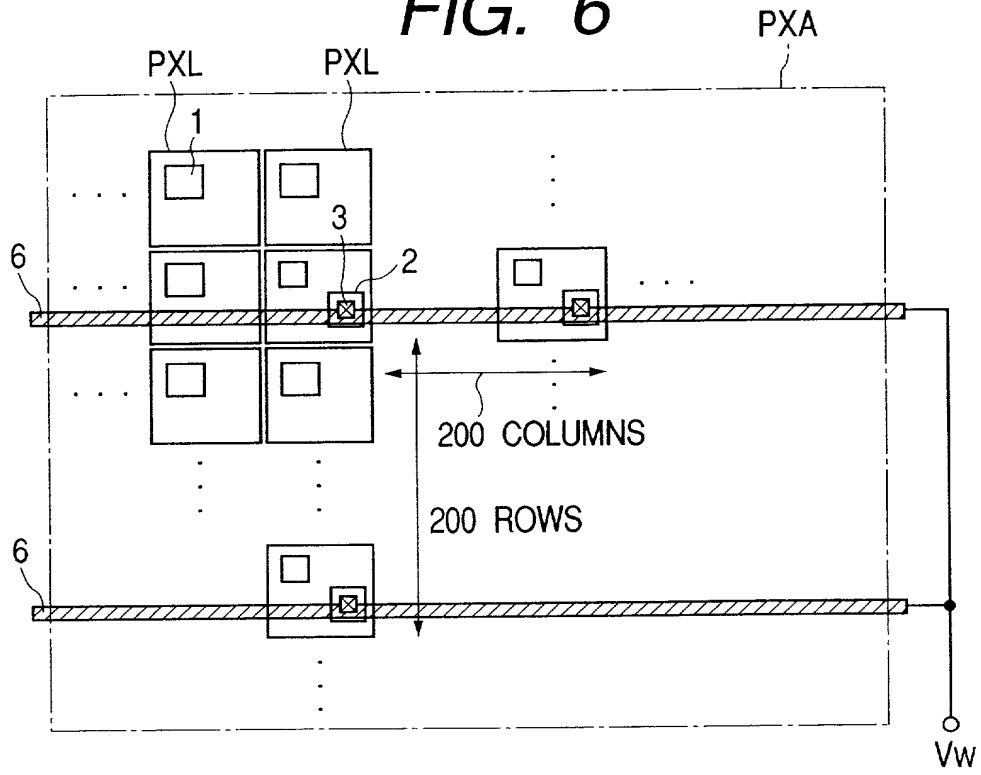


FIG. 5



**FIG. 6**



**FIG. 7**

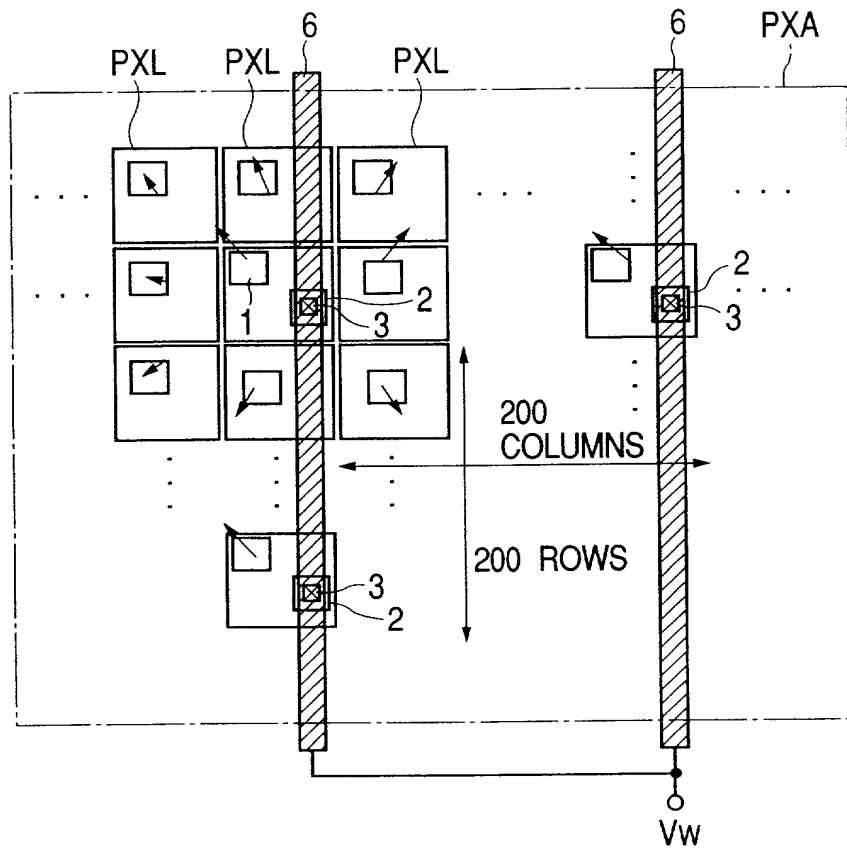


FIG. 8

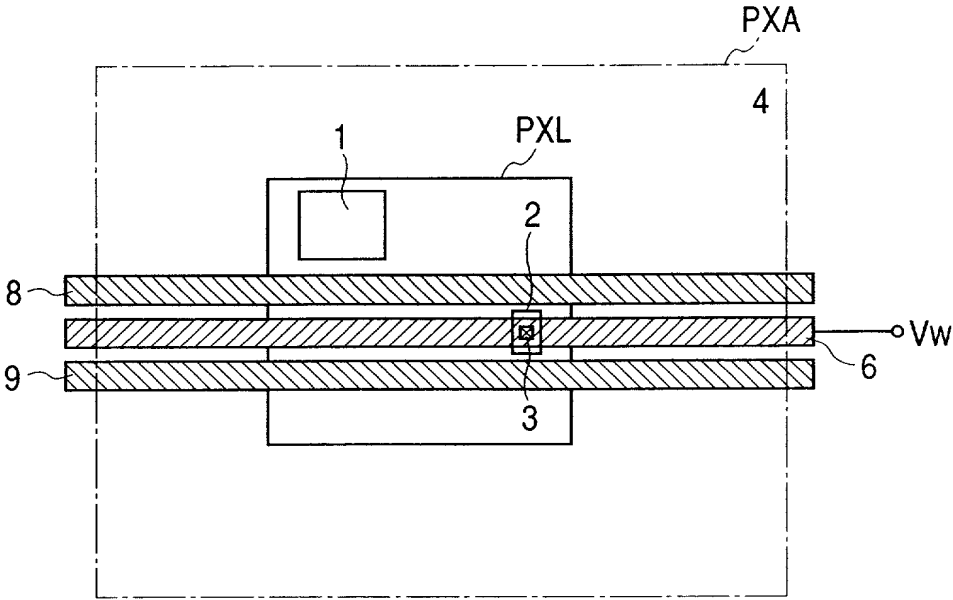
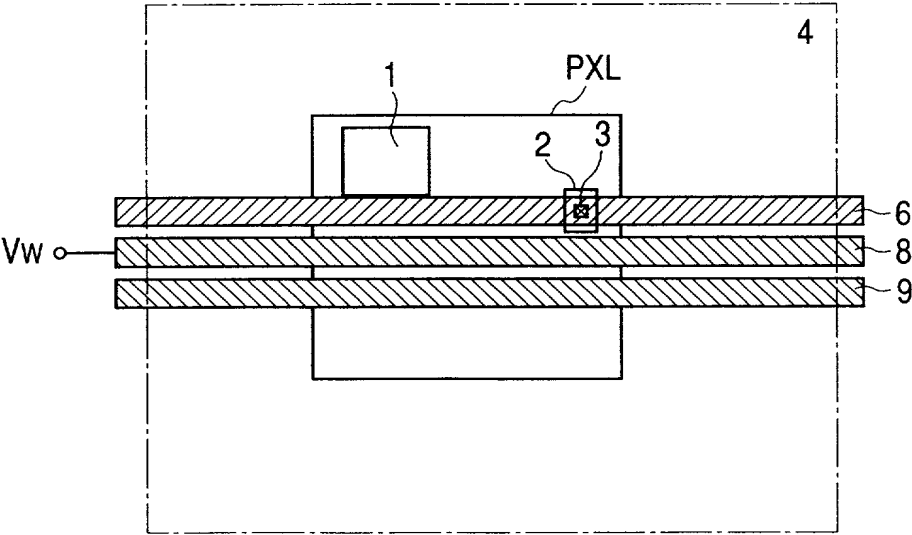
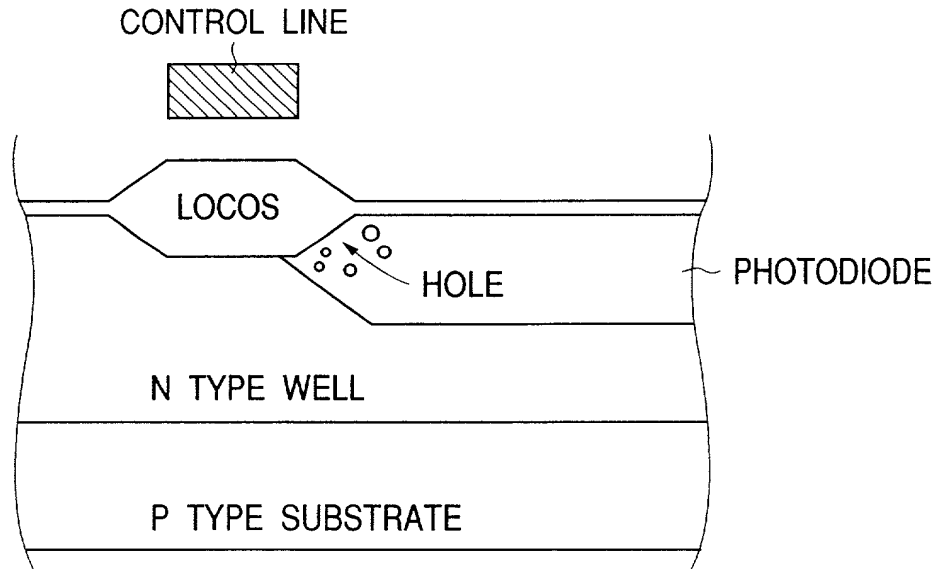


FIG. 9





**FIG. 10A**



**FIG. 10B**

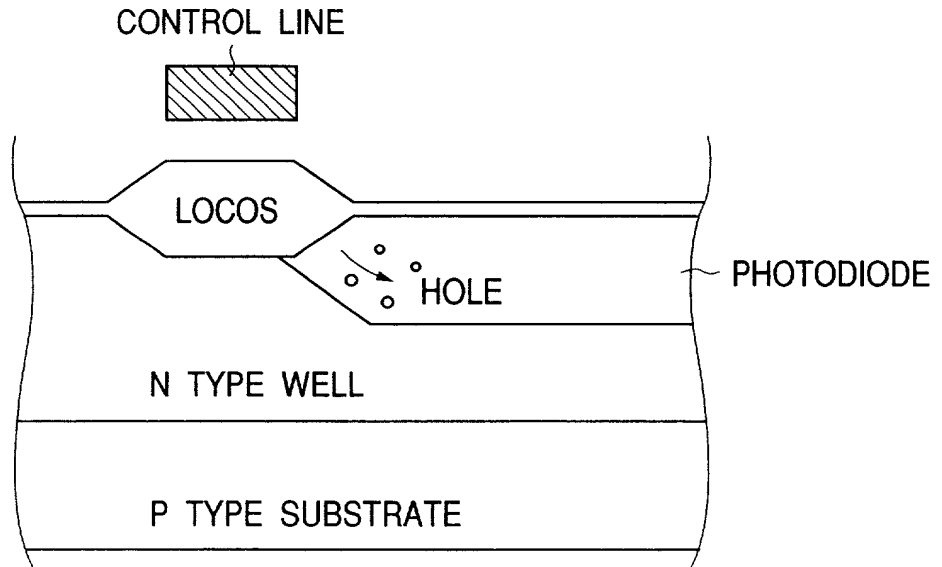


FIG. 11

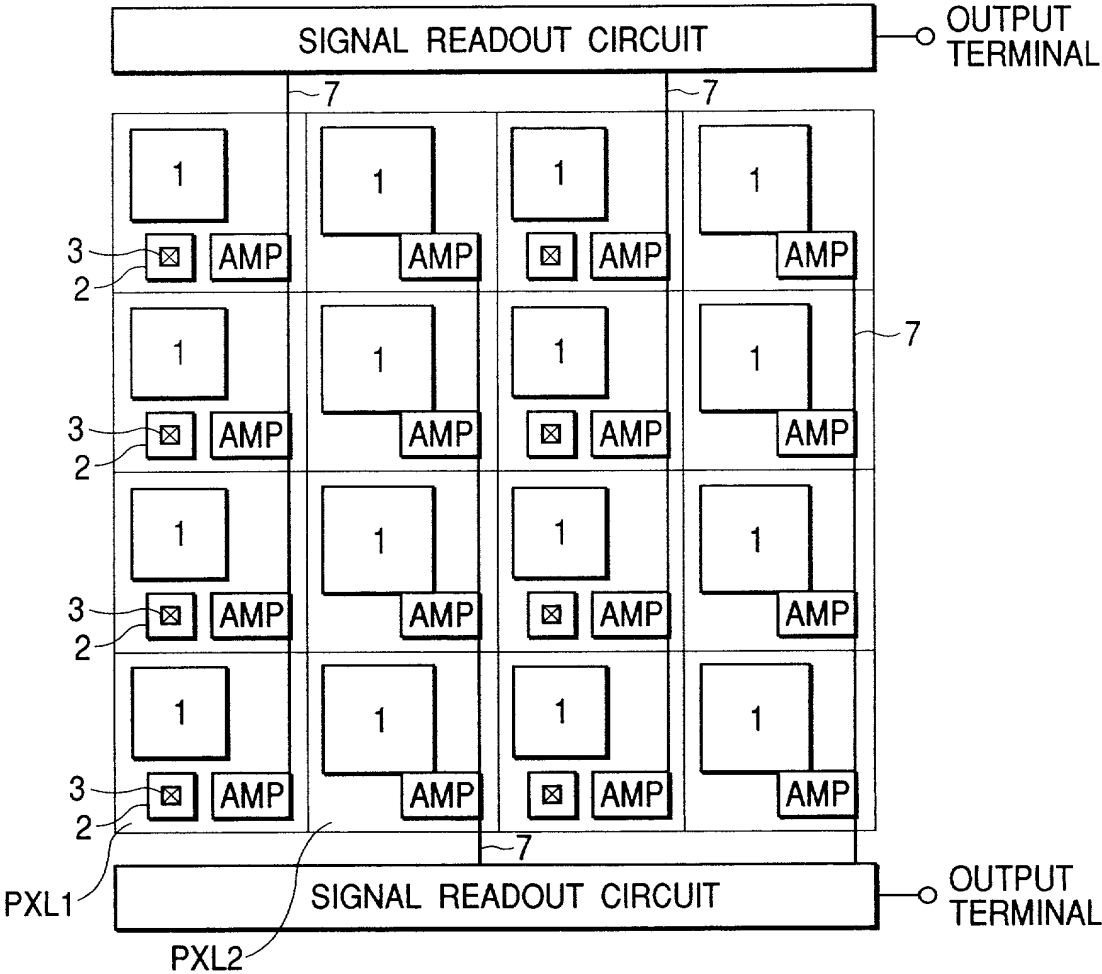


FIG. 12

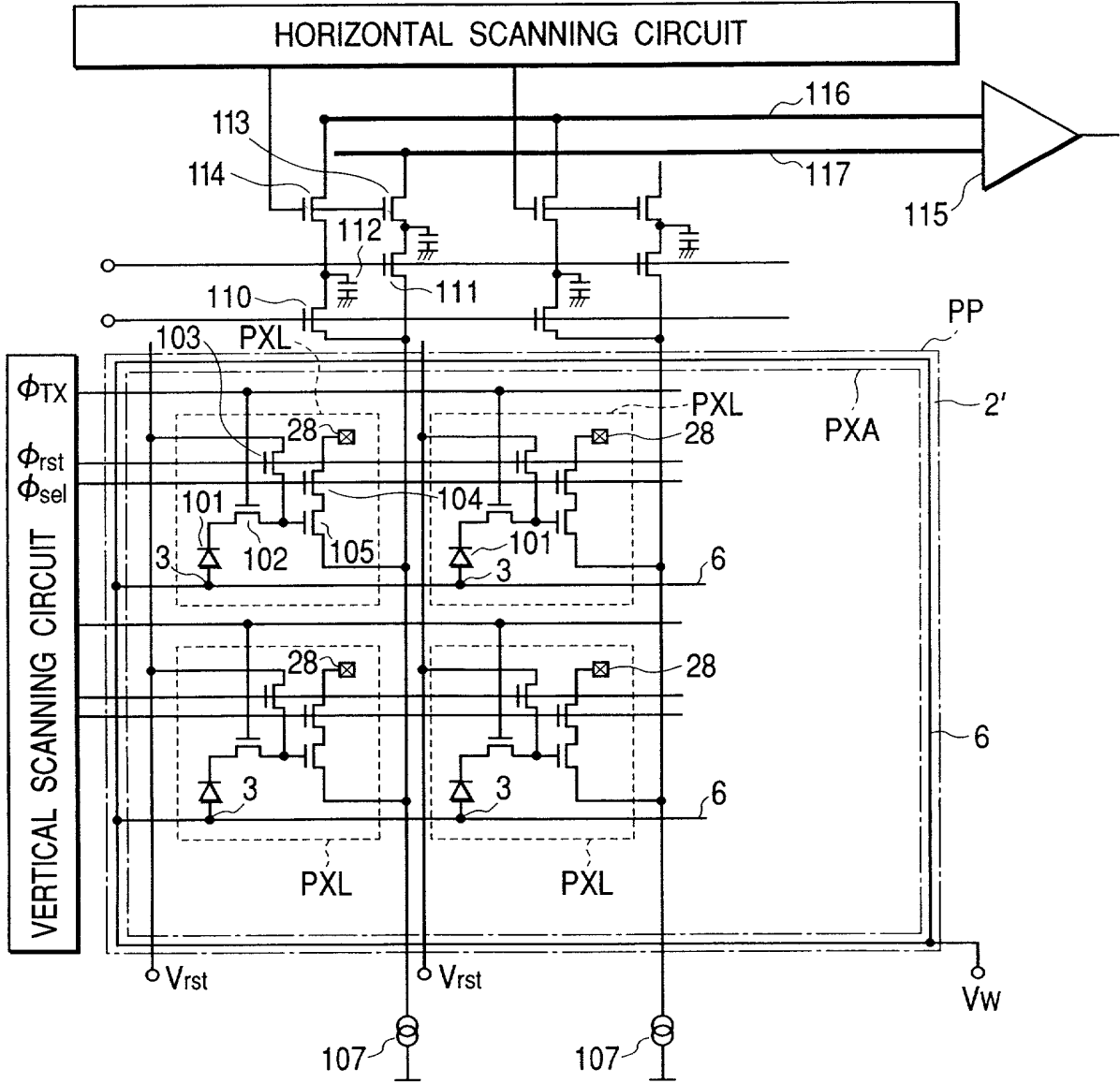
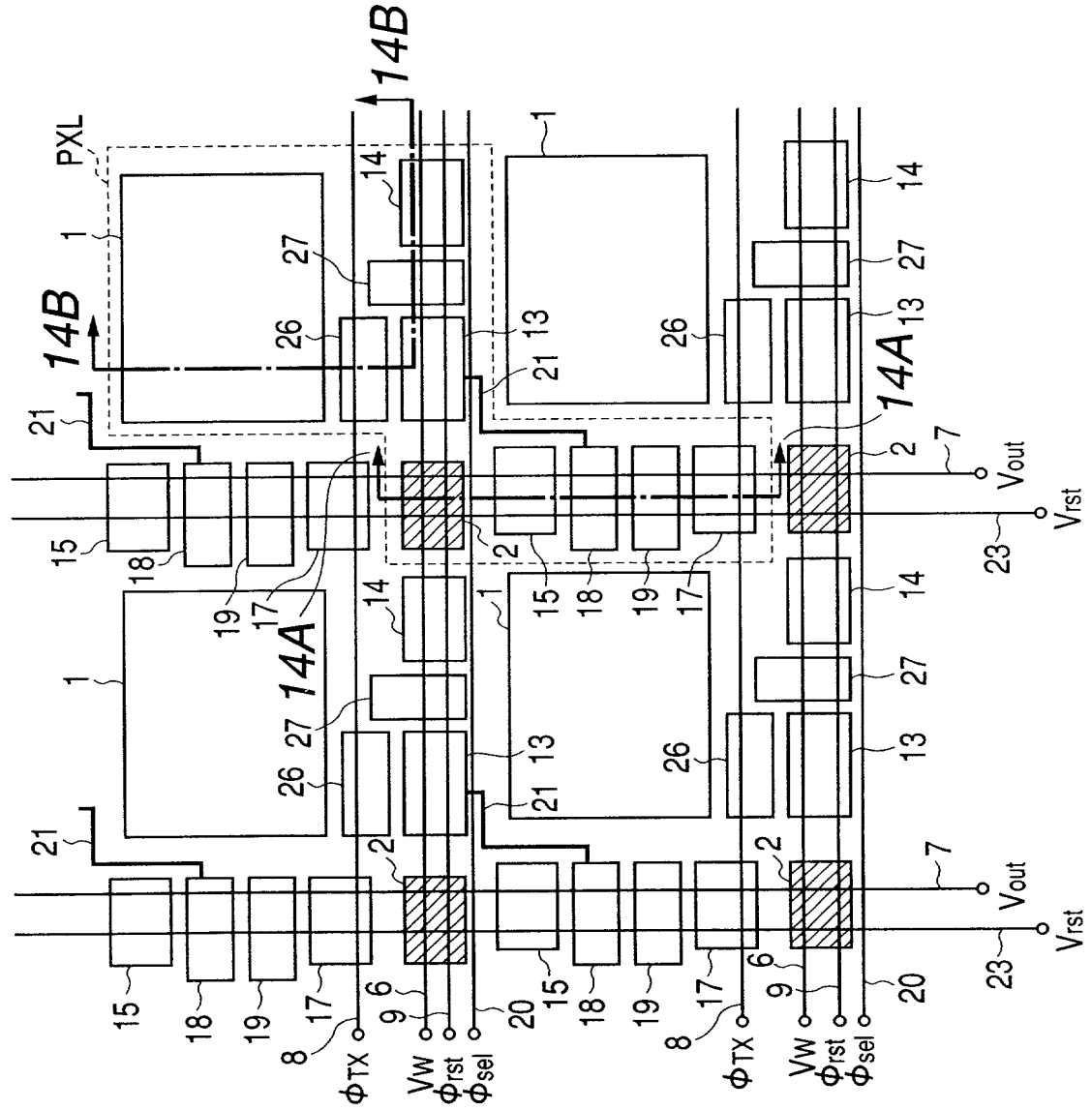
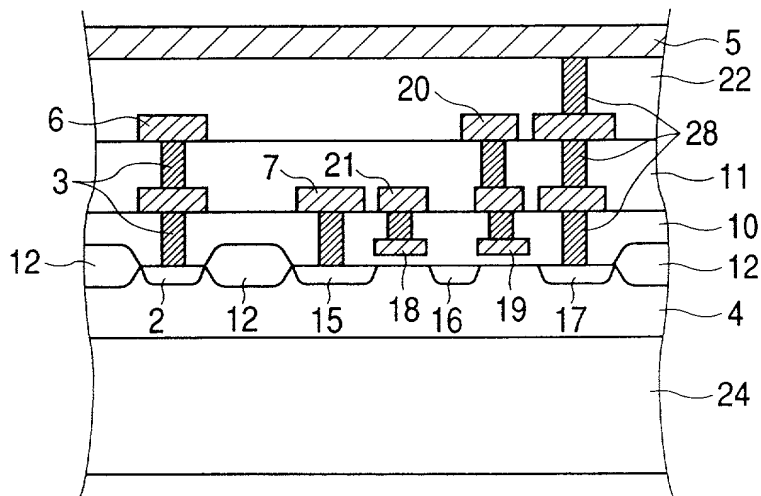


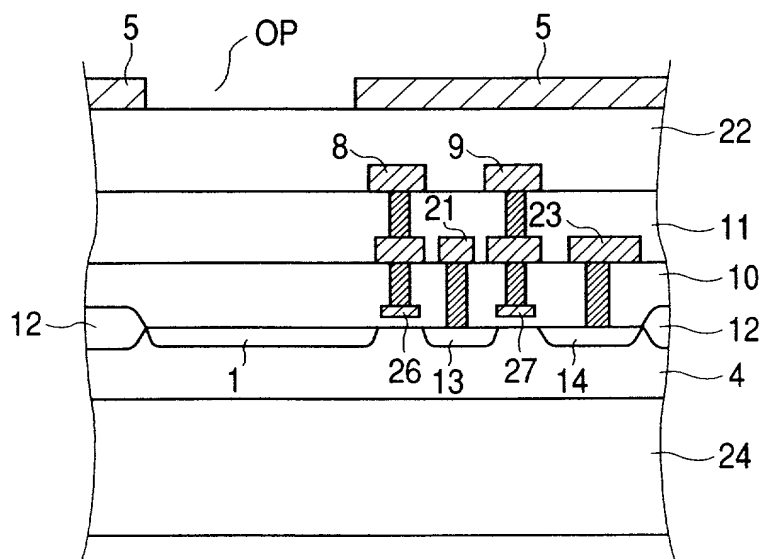
FIG. 13



**FIG. 14A**



**FIG. 14B**



**FIG. 15**

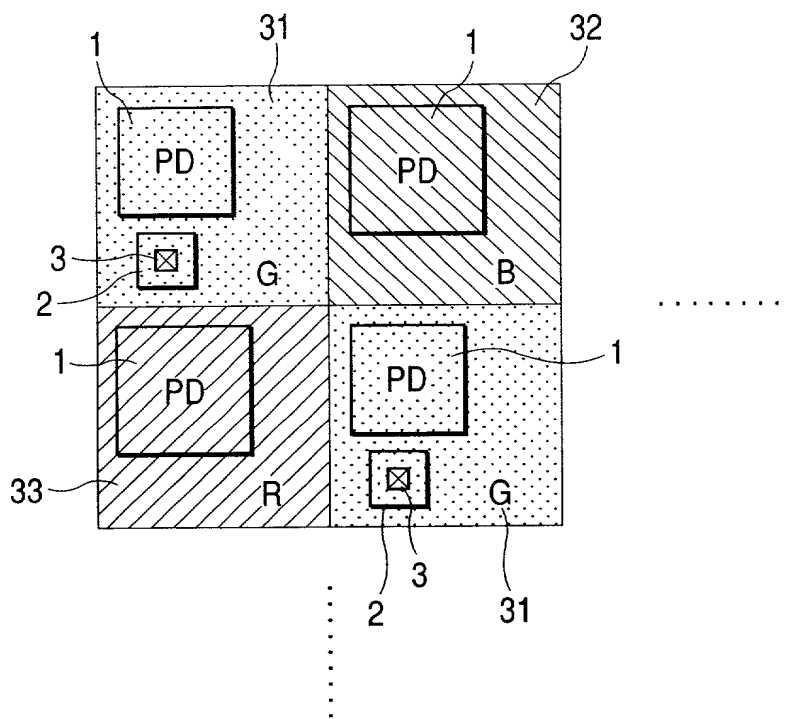
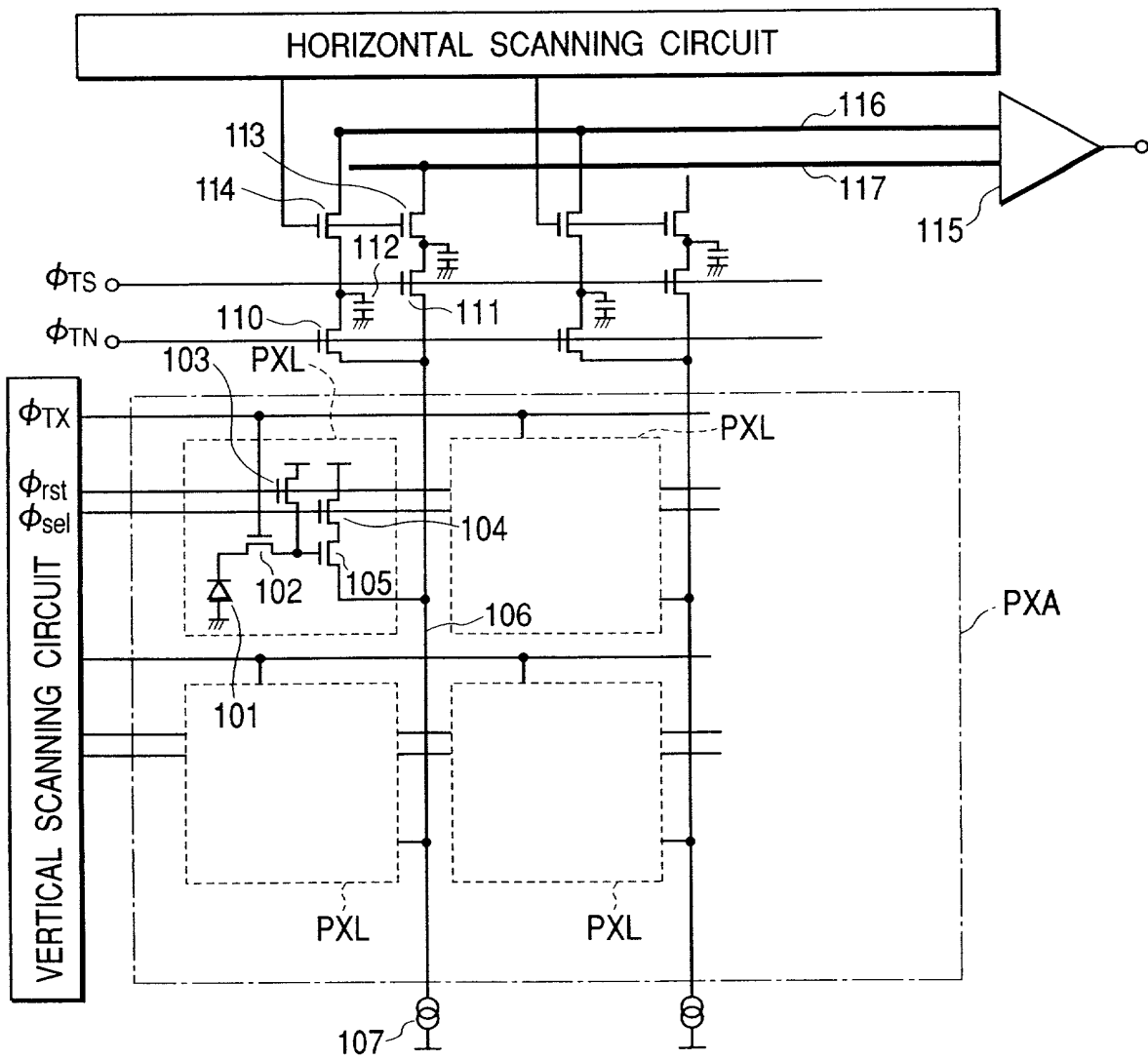


FIG. 16



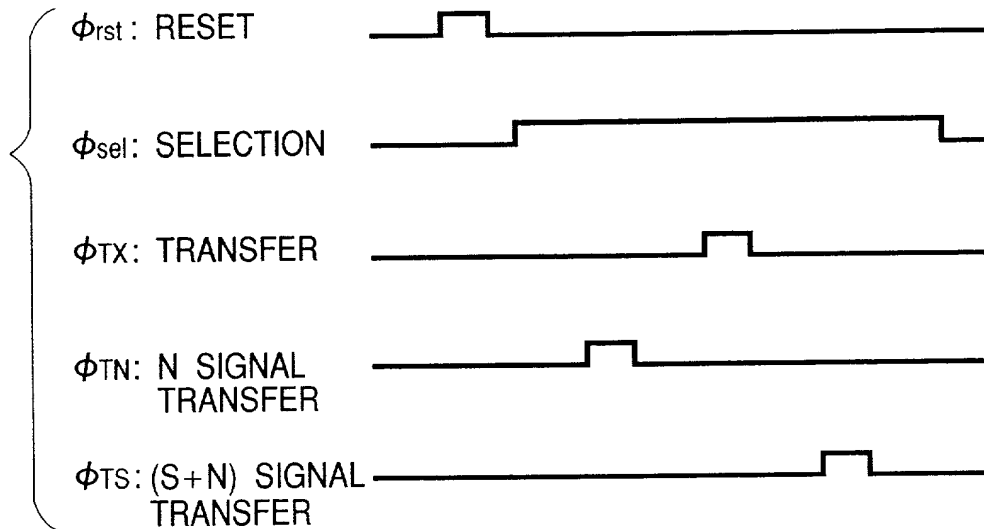
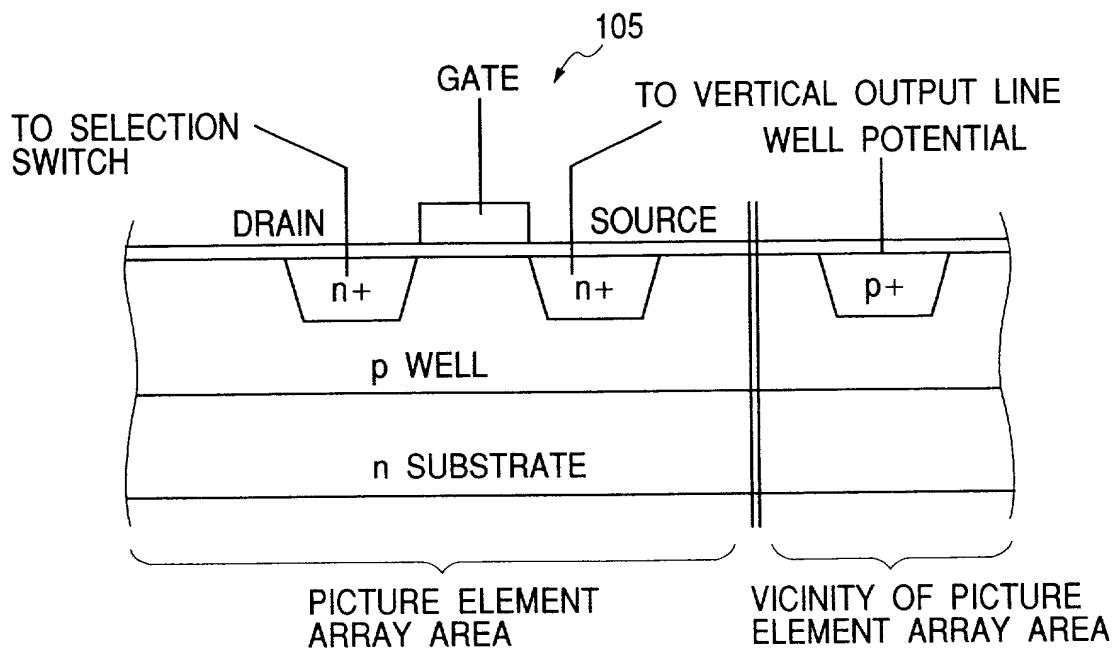
**FIG. 17****FIG. 18**



FIG. 19A

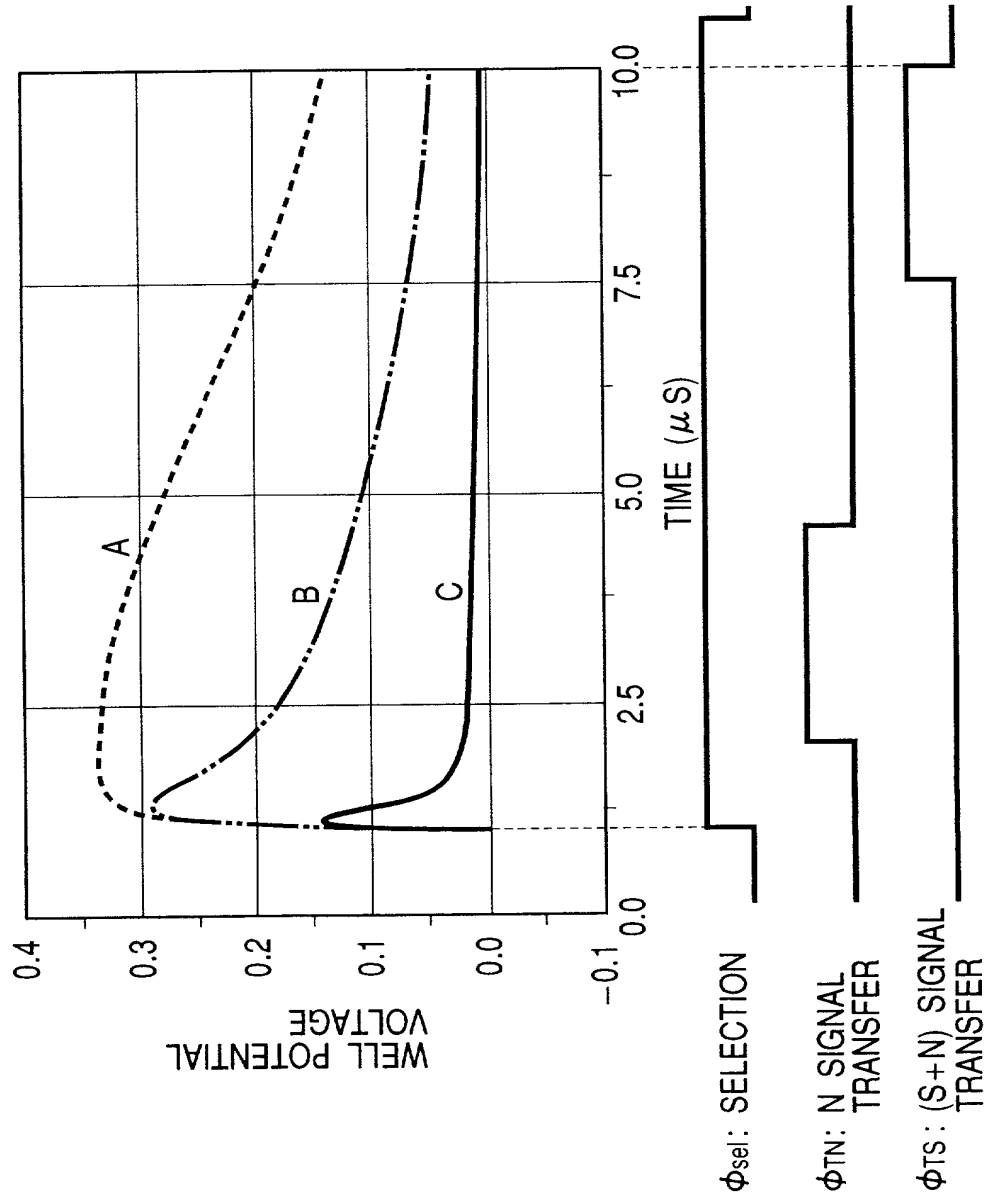
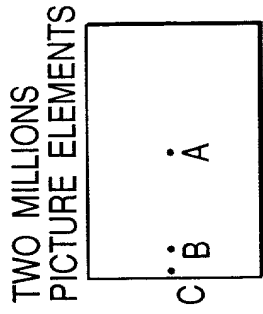


FIG. 19B



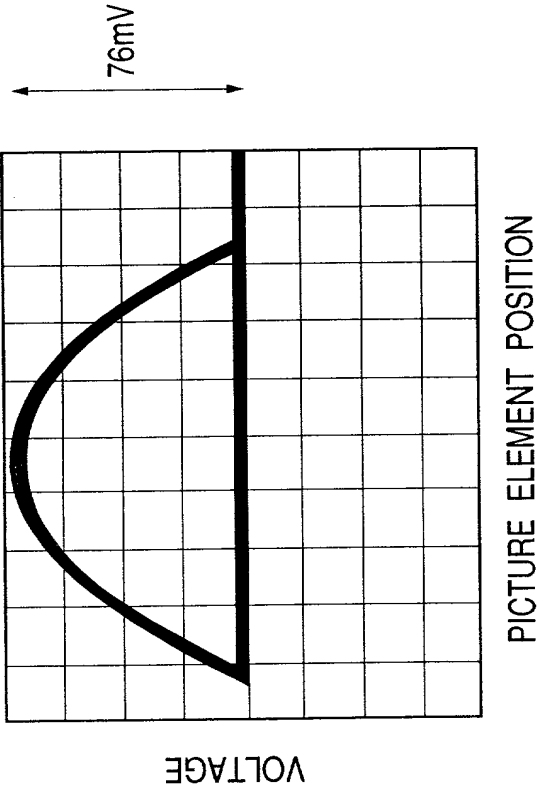


FIG. 20

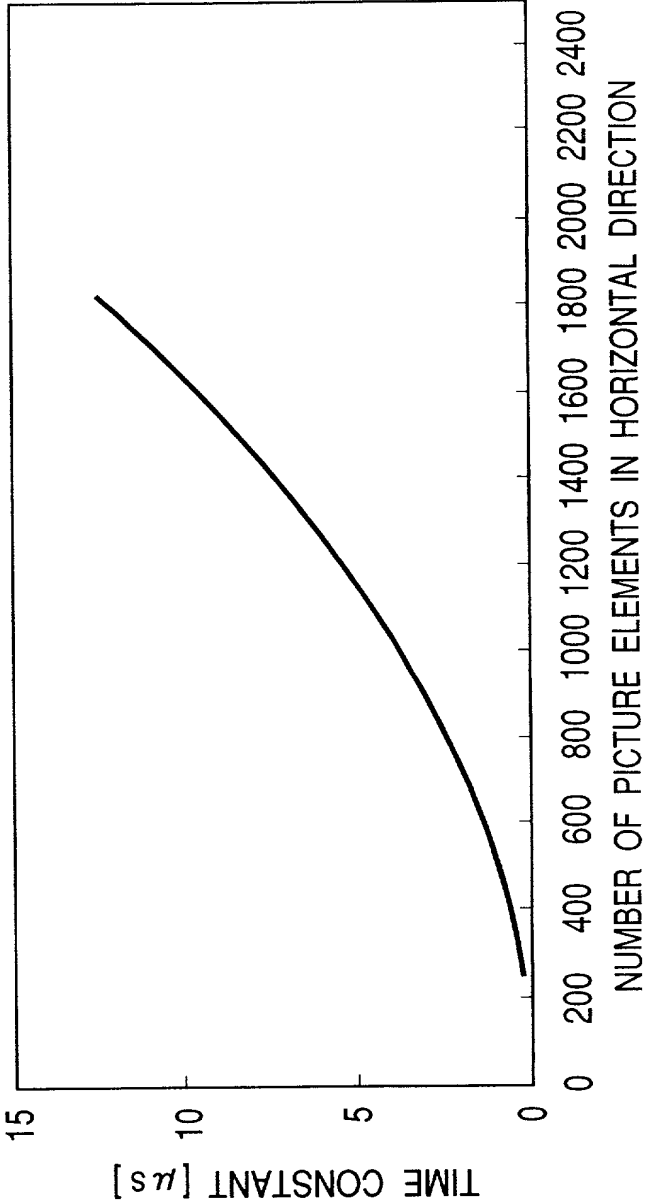


FIG. 21